Comparison of the behavior of Voltage Mode, V^2 and V^2I_c control of a buck converter for a very fast and robust dynamic response

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***Abstract*—This paper proposes an optimization method to design the parameters of controls for power converters in order to achieve a very fast dynamic response while remaining stable and robust over the desired operation region. The proposed optimization algorithm is applied to different analog controls and is used to compare the dynamic response of the Voltage mode, V^2 and V^2I_c control for different cases in order to evaluate which control presents the best performance in terms of dynamic response and stability robustness to system tolerances.**

***Index Terms*—control of DC/DC converters, fast, robustness, voltage mode, v2, v2ic, optimization.**

I. Introduction

Increasingly demanding loads and applications requiring voltage reference tracking have lead the industry and academics to develop novel controls in order to achieve a very fast dynamic response for Buck converters. But thorough comparison between control alternatives is lacking.

In the case of digital controls, the Minimum Time control [1], [2] and the Centric-based control [3] can achieve the best possible dynamic response, although tolerances of the converter and parasitic elements limit their performance in real-world applications. Novel digital controls should be compared to them or to the benchmark limits derived from the Natural Trajectories [4] that the Centric-based control uses.

But, in some cases, analog controls are preferable because of simplicity or because the switching frequency is too high to allow digital control. In [5], the dynamic response of different modulation techniques are evaluated by exploring their small-signal characteristics. However, it seems more appropriate to study the large-signal behavior of the controls.

The comparison of different analog controls is not easy as the tuning of the different parameters of the control can greatly vary the dynamic response of the control. Furthermore, the power stage plays a critical role in the dynamic behavior. Consequently, a control could behave very well in a certain design with a big output capacitor and worse with a smaller output capacitor. Therefore, the designer of power converters does not have a clear view of the possibilities of each control.

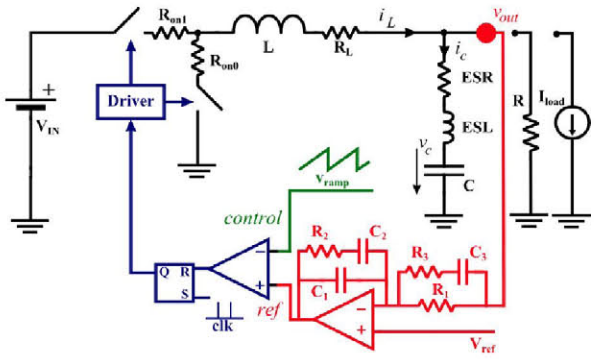
This paper proposes an algorithm to optimize the parameters of different controls of power converters which, not only optimizes the dynamic response of the control for the nominal case, but assures stability over a wide rage of conditions. Specifically, the algorithm assures stability under the whole operating region and under variations of passive elements due to tolerances. It is based on Discrete Modeling to compute the large-signal behavior and in the Floquet Theory to evaluate the stability of the converter at several points of operation. With this method, a comparison of the optimized dynamic responses of Voltage Mode, V^2 and V^2I_c control is carried out to evaluate which control is more suitable for each specification.

The paper is organized as follows: section II reviews the fundamentals of Voltage mode, V^2 and V^2I_c control, section III compares the controls based on a proposed optimization algorithm and discusses the results, section IV validates experimentally the designs obtained from the optimization algorithm and section V summarizes the comparison of the controls and provides some conclusions derived from the study. All the simulation results shown in the paper are obtained from the program Simplis.

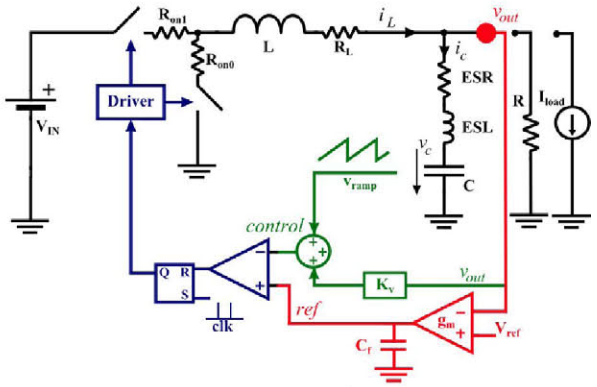
II. Review of Voltage mode, V^2 and V^2I_c control

Voltage mode control, fig.1a, is the most common approach to control a buck converter. It only employs a linear controller to regulate the ouput voltage and a ramp signal to create the PWM. A type-III controller is usually used in order to boost the phase at the crossover frequency.

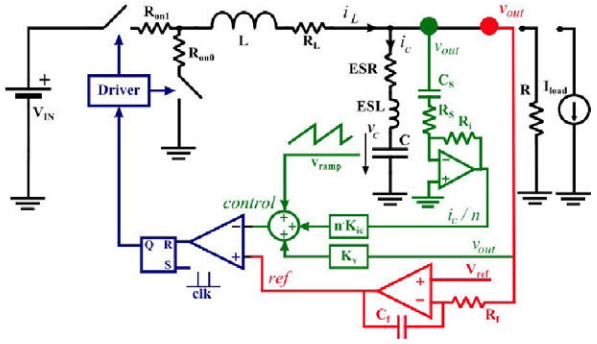
V^2 [6], fig.1b, is a ripple-based control that uses the output voltage as the triangular signal for the PWM. As a



(a) Constant frequency Voltage Mode control.



(b) Constant frequency V^2 peak control.



(c) Constant frequency V^2I_c peak control.

Fig. 1: Architecture of different analog controls with fixed frequency modulation.

consequence, when the converter is perturbed with a load disturbance, the output voltage changes which changes the duty cycle and the system is able to react very fast. A compensating ramp can be added to help to stabilize the converter [7].

V^2I_c [8], fig.1c, is also a ripple-based control that uses both the output voltage and the current through the output capacitor as the triangular signal for the PWM. As the current through the output capacitor is the inductor current minus the output current, this control presents inherently a feed-forward of the output current and, thus, it is very fast under load disturbances. The current through the output capacitor is sensed indirectly by means of a trans-impedance amplifier [9] in order not to introduce losses in the converter. The reference [10] presents an accurate small-signal model of a simplified version of V^2I_c.

III. Comparison of Voltage mode, V^2 and V^2I_c

This section compares the dynamic response under load disturbances and voltage reference steps of Voltage mode, V^2 and V^2I_c control with constant frequency modulation. The comparison is done for several sizes and technologies of output capacitors: a $300\mu F$ OS-CON cap, a $300\mu F$ ceramic cap and a $30\mu F$ ceramic cap. The section is divided in three subsections where:

- subsection III-A explains the proposed optimization algorithm to design controls of power converters. This method is used later to optimize the controls of the comparison for a very fast and robust dynamic response.
- subsection III-B shows the optimized responses of the controls and subsection III-C discusses the results.
- subsection III-D shows how a Voltage mode control can behave very fast but with poor robustness. This is interesting for systems where the tolerances of the passives are very narrow and, therefore, inherently robust.

A. Proposed optimization algorithm

The proposed optimization algorithm uses the Discrete modeling to compute the dynamic behavior of the converter and the Floquet theory to analyze its stability.

The dynamic behavior of power converters can be accurately modeled by means of Discrete Modeling together with Floquet theory [11]. Not only a discrete model of the form of $x_{k+1} = f(x_k)$ can be derived but the whole time-domain waveform can be reconstructed. The stability of the power converter can be analyzed by means of the Floquet theory which is able to predict sub-harmonic oscillations [11]. The major advantages of these techniques are the accuracy, the simplicity of including parasitic elements and the extension of the methodology to other controls. Notice in fig.1 that the converters present all the significant parasitic elements, the passives of the linear controller and even the real current sensor of V^2I_c to evaluate mismatches. The models used in the algorithm contain all these parameters in order to assure robustness.

Figure 2 shows a conceptual scheme of the optimization algorithm. In order to design robust controls of power converter, not only the dynamic behavior at nominal operation needs to be optimized but the system needs to be stable and within dynamic requirements over all the desired region of operation and under changes in the value of parameters of the power stage due to tolerances. This means that the stability needs to be assessed at different conditions. Also, the values of the passive elements need to be implementable in practice. The optimization process takes into account all these and reject the solutions that do not comply with the requirements. Consequently, the final design of the control is both fast and robust.

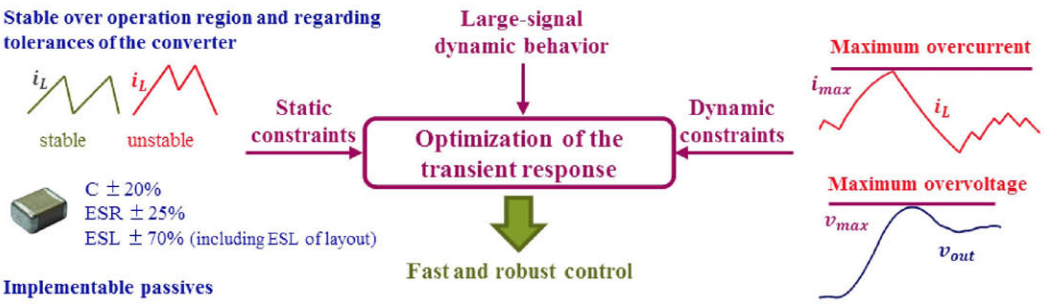


Fig. 2: Proposed optimization algorithm of the transient response taking into account static and dynamic constraints.

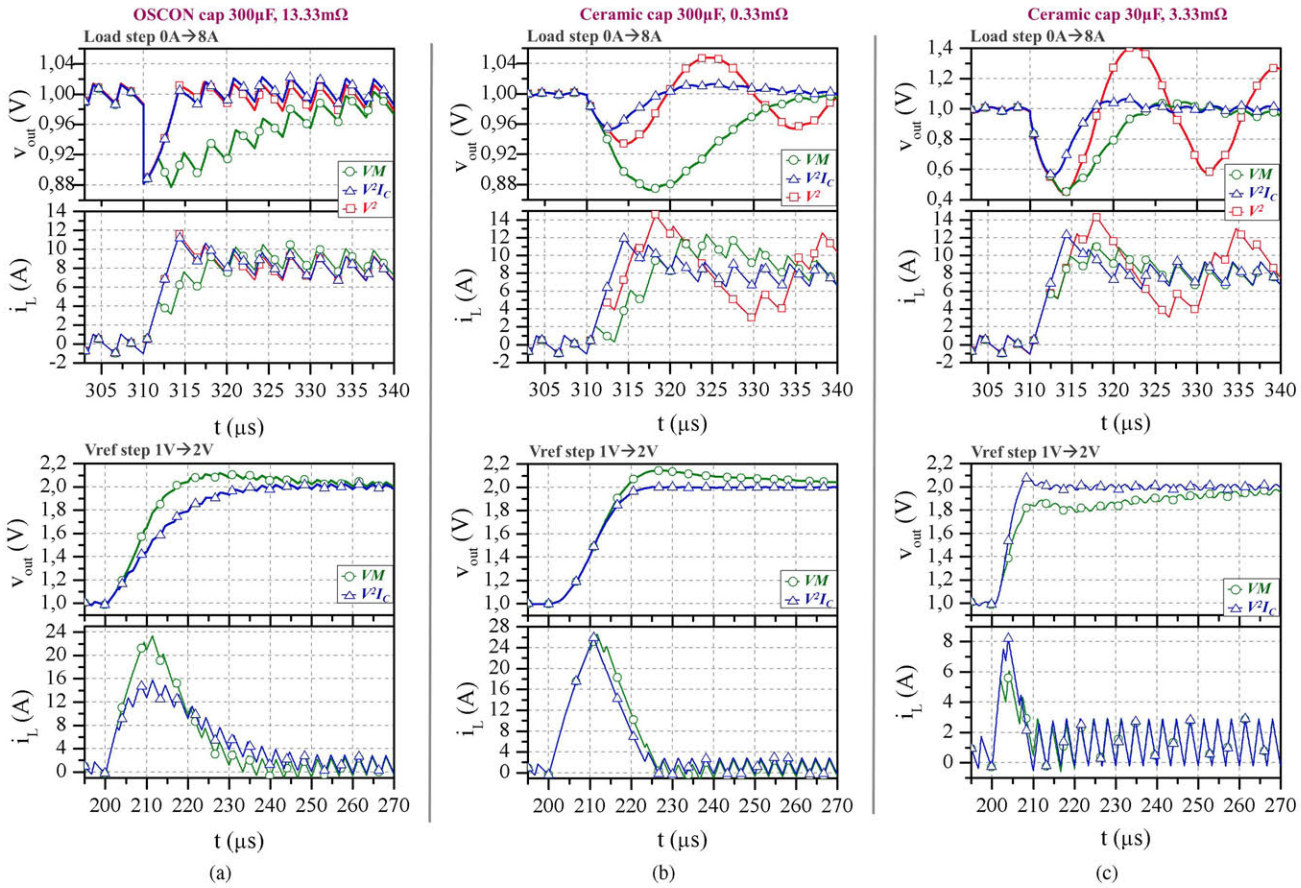


Fig. 3: Comparison of the dynamic behavior of Voltage mode, V^2I_c and V^2 under voltage reference steps and load steps for different size of capacitors and capacitors technologies. Voltage reference step $1V \rightarrow 2V$ (upper graphs). Load step $0A \rightarrow 8A$ (lower graphs).

B. Results

The power stage of the Buck converter is as follows: $F_{sw} = 300kHz$, $V_{in} = 5V$, $V_{out} = 1V \leftrightarrow 2V$, $I_{out} = 0A \leftrightarrow 8A$, $L = 1.3\mu H$. The discrete model also includes the ESR and ESL of the output capacitor (specified later for each case), the on-resistances of the switches ($50m\Omega$) and the ESR of the inductor ($10m\Omega$).

Each control is designed for a fast and robust dynamic response possible using the proposed methodology. The optimization algorithm is setup in the following way:

- Voltage mode and V^2I_c are optimized for load disturbances and voltage reference steps whereas V^2 is only optimized for load steps as it is very slow under voltage reference steps.
- The converter needs to be stable over the whole operation region and accounting for tolerances of the passive elements. The operation region is as follows: the output voltage can vary from 1V to 4V and the output current can vary from 0A to 10A. The tolerances of the passive elements are as follows: for the output capacitor, $C \pm 20\%$, for the inductor, $L \pm 20\%$, and for the ESL of the output capacitor, $ESL \pm 70\%$. It is important to point out that the ESL considers also the additional inductance introduced by the layout and, consequently, the range of variation of

the ESL can be large.

- Only capacitance values greater than $10pF$ are allowed in the linear controllers so that the design is implementable in practice.

Fig.3 shows the comparison of the dynamic response under voltage reference steps and load steps of the voltage mode, V^2 and V^2I_c control for different sizes of capacitors and different capacitor technologies. An OS-CON capacitor of $300\mu F$ is used in fig.3a, a ceramic capacitor of $300\mu F$ is used in fig.3b and a ceramic capacitor of $30\mu F$ is used in fig.3c. The results are obtained from the program Simplis.

C. Discussion

First, examine the dynamic response of V^2I_c under the positive voltage reference step in fig.3b and fig.3c. The control commands a lengthy on-time and then a lengthy off-time to reach steady-state without overshooting. These transients are very similar to the transient response of the digital Minimum time control [1],[2] which is the fastest that can be done to reach the steady-state. This shows that the controls are truly optimized which gives more value to the comparison.

The evaluation of the comparison is as follows:

- Voltage mode achieves a good dynamic response under voltage reference step. Under the load step, the voltage drop is larger than in the case of the other controls but it can be acceptable.
- V^2 exhibits a very slow dynamic response under voltage reference step so fig.3 does not include the V^2 control for the voltage reference steps. Under load steps, V^2 reacts extremely fast for high capacitance values and high ESR, recovering from the load step in one clock cycle. For ceramic capacitors, the converter oscillates under a load step achieving a very poor response time. As seen, a good transient response cannot be reached with V^2 control with a low ESR capacitor. In order to improve the dynamic response, current information has to be added to the fast loop. The current information can be the inductor current, what is known as V^2 with hybrid ramp compensation [12], or the current through the output capacitor, what is then known as V^2I_c control.
- V^2I_c achieves the overall best response of all controls. It achieves an excellent dynamic behavior under voltage reference steps and under load steps for low and high capacitance values.

D. A very fast voltage mode control

For the comparison of the previous section, the optimization is set up to design a fast and robust control by taking into account a stability analysis over the whole operating region and regarding tolerances of the system. Specifically, recall that the optimization assured stability for changes in the value of the output capacitor and in the inductor of $\pm 20\%$ over the nominal value. For these tolerances, the transient response of V^2I_c is better than the transient response of Voltage mode.

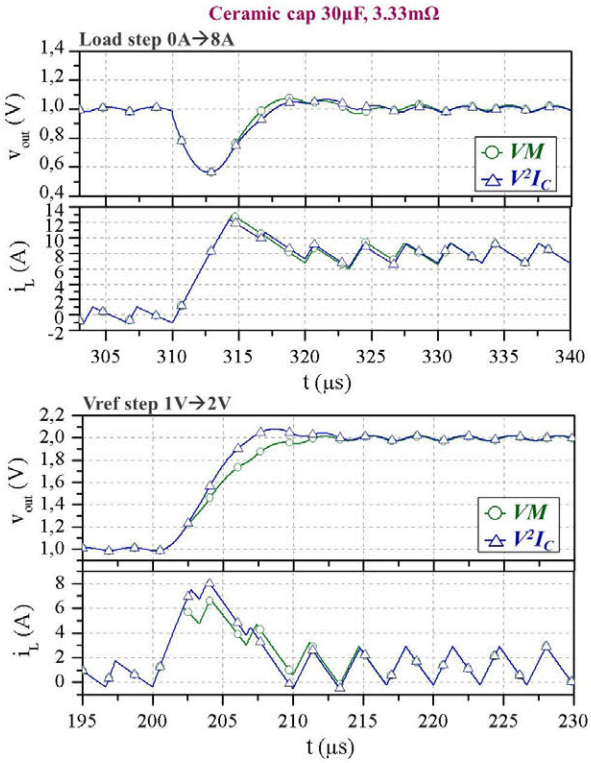
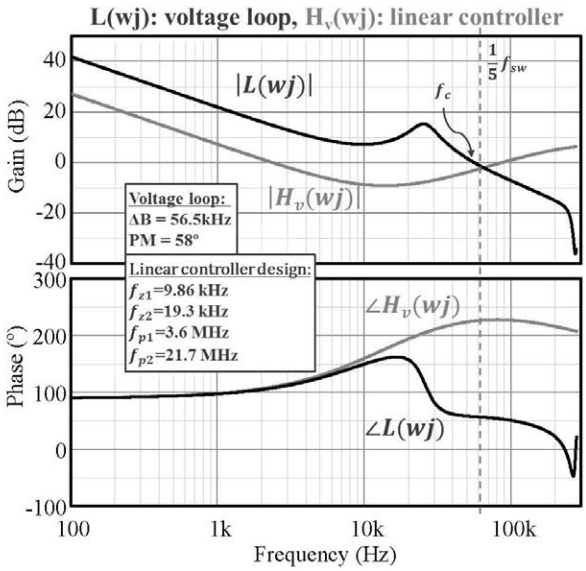


Fig. 4: Comparison of the dynamic behavior of Voltage and V^2I_c under voltage reference steps and load steps. Optimized assuming very narrow tolerances of passive elements.

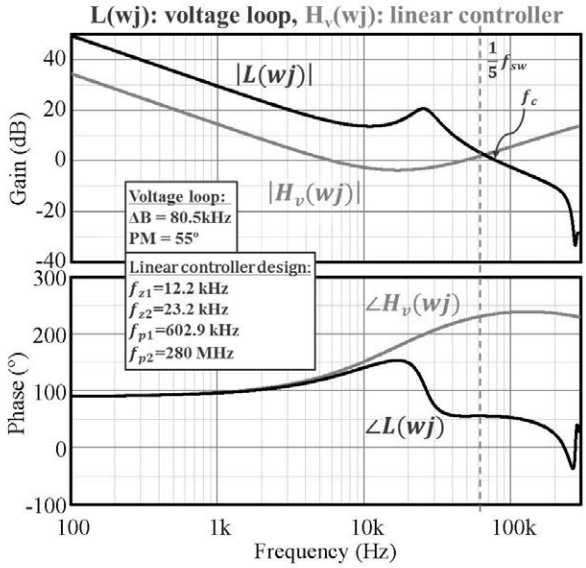
Now, a new comparison is carried out assuming a very narrow tolerance of the passive elements. Figure 4 compares the Voltage mode and V^2I_c controls optimized assuming a tolerance of only $\pm 5\%$ in the value of the output capacitor and the inductor. Notice that the response of V^2I_c is the same as in fig.3c where tolerances of $\pm 20\%$ are assumed. This means that the fast dynamic response of V^2I_c is very robust. Notice also that, now, Voltage mode control achieves almost the same response as V^2I_c control.

Figure 5 shows the Bode diagram of the linear controller and the voltage loop of the two designs of Voltage mode control. The first Bode plot (fig.5a) corresponds to the robust design of fig.3c. The phase margin is 58^o and the bandwidth of the control is $56.5kHz$, just below $f_{sw}/5$. The second Bode plot (fig.5b) corresponds to the robust design of fig.4. The phase margin is 55^o and the bandwidth of the control is $80.5kHz$, above $f_{sw}/5$. This frequency is commonly a practical limit in the design of the bandwidth of linear controllers.

Several conclusions can be derived from this section. First, V^2I_c exhibits a very fast and robust dynamic response. On the other hand, Voltage mode control needs to be slower in order to be robust. In the case that the tolerances of the passives are narrow and, therefore, the system is inherently robust, Voltage mode control can achieve an excellent dynamic response.



(a) Design A: robust Voltage mode control of fig.3c.



(b) Design B: very fast Voltage mode control with poor robustness of fig.4.

Fig. 5: Bode plots of two different designs. The Voltage loop transfer function, $L(wj)$, is shown in black and the transfer function of the linear controller, $H_v(wj)$, is shown in grey. The figures also show the corresponding bandwidth and phase margin of the loop gain and the poles and zeros of the controllers.

IV. Experimental validation

This section validates the optimized designs of a Voltage mode and V^2I_c of a $300kHz$ Buck converter to prove that the designs of the proposed optimization algorithm that is used in the comparisons are feasible. The Buck converter has the following specifications: $F_{sw} = 300kHz$, $V_{in} = 5V$, $v_{out} = 1V \leftrightarrow 2V$, $I_{out} = 0A \leftrightarrow 8A$, $C = 40\mu F$, $L = 1.3\mu H$. The power stage also includes the ESR ($4m\Omega$) and ESL ($600pH$) of the output capacitor, the on-resistances of the switches ($30m\Omega$ for the high-side MOSFET and $14.2m\Omega$ for the low-side MOSFET) and the ESR of the inductor ($15m\Omega$).

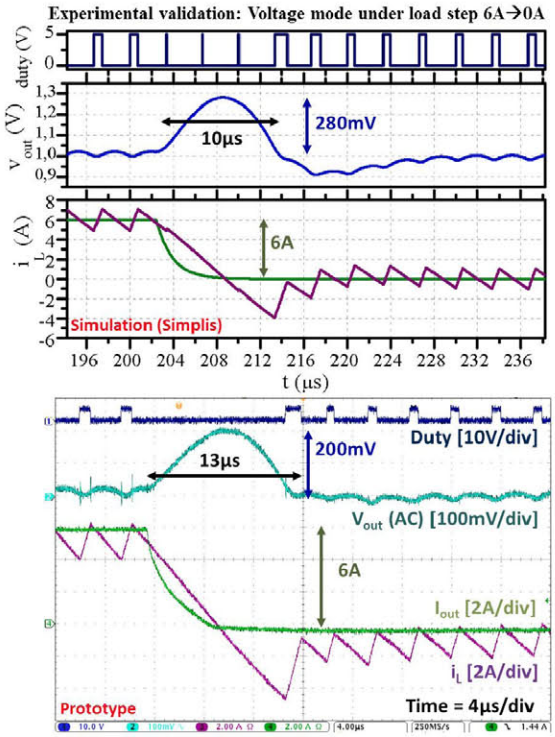
Each control is designed for a fast and robust dynamic response possible using the proposed methodology. The optimization algorithm is setup in the following way:

- The controls are optimized for load disturbances and voltage reference steps.
- The converter needs to be stable over the whole operation region and accounting for tolerances of the passive elements. The operation region is as follows: the output voltage can vary from 1V to 4V and the output current can vary from 0A to 10A. Only the tolerance of the ESL of the output capacitor is taken into account, which is $ESL \pm 70\%$.
- Only capacitance values greater than $10pF$ in the linear controllers are allowed so that the design is implementable in practice.

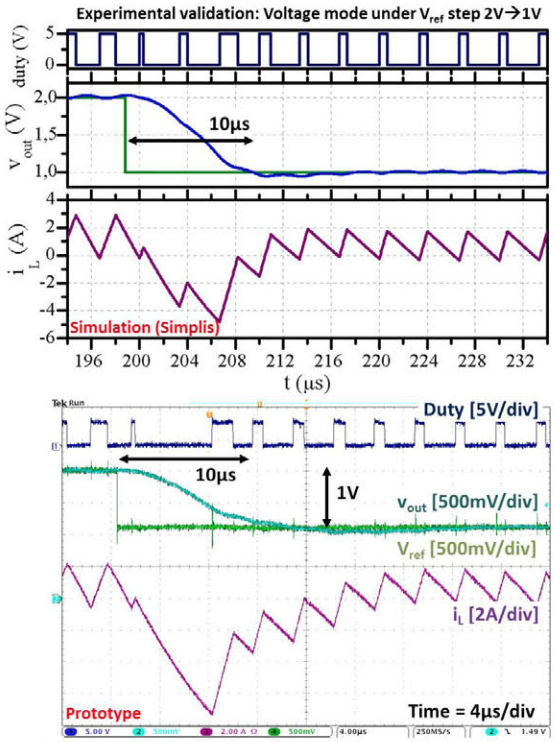
Notice that the tolerances of the capacitor and the inductor are not considered in the optimization algorithm. This is because when the stability under variations of the power stage is not considered, a very fast Voltage mode control is designed (refer to subsection III-D). Therefore, it is very interesting to validate the feasibility of this very fast Voltage mode control.

Figures 6a and 6b show the experimental validation of the Voltage mode control. The figure shows the transient response under a negative voltage reference step from $2V$ to $1V$ and a negative load step from $6A$ to $0A$. The converter is able to react within three clock cycles both in simulation results and in the experimental prototype, validating that the Voltage mode control designed with the proposed optimization methodology can be implemented in practice and achieves very fast transient responses.

Figures 7a and 7b show the experimental validation of the V^2I_c control. The figure shows the transient response under a negative voltage reference step from $2V$ to $1V$. The converter is able to react within three clock cycles both in simulation results and in the experimental prototype, validating the V^2I_c design that the optimization algorithm yields.

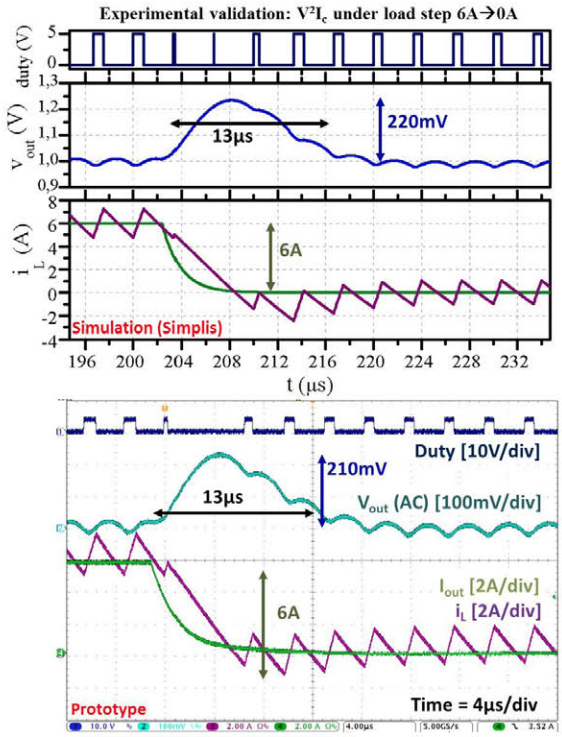


(a) Voltage mode under load step $6A \rightarrow 0A$. Simulation results (upper) and experimental validation (lower).

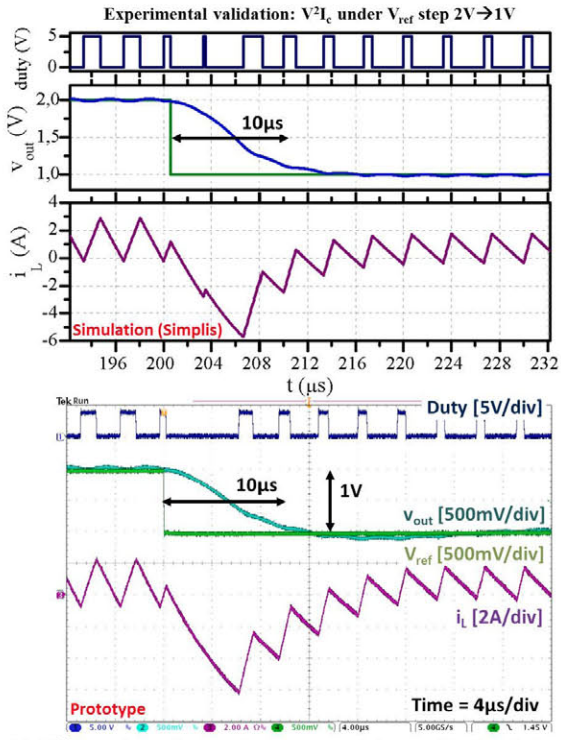


(b) Voltage mode under voltage reference step $2V \rightarrow 1V$. Simulation results (upper) and experimental validation (lower).

Fig. 6: Experimental validation of the optimized design of Voltage mode control of a 300kHz Buck converter. Load step (a) and voltage reference step (b).



(a) V^2I_c under load step $6A \rightarrow 0A$. Simulation results (upper) and experimental validation (lower).



(b) V^2I_c under voltage reference step $2V \rightarrow 1V$. Simulation results (upper) and experimental validation (lower).

Fig. 7: Experimental validation of the optimized design of V^2I_c control of a 300kHz Buck converter. Load step (a) and voltage reference step (b).

TABLE I: Summary of the comparison of the dynamic behavior of Voltage mode (VM), V^2 and V^2I_c control for different output capacitors. Tolerances considered: $L \pm 20\%$, $C \pm 20\%$, $ESL \pm 70\%$.

	LOAD STEP			**VOLTAGE REFERENCE STEP**		
	OSCON $\mathbf{C = 300\mu F}$ $\mathbf{ESR = 13.3m\Omega}$	**CERAMIC** $\mathbf{C = 300\mu F}$ $\mathbf{ESR = 0.3m\Omega}$	**CERAMIC** $\mathbf{C = 30\mu F}$ $\mathbf{ESR = 3.3m\Omega}$	**OSCON** $\mathbf{C = 300\mu F}$ $\mathbf{ESR = 13.3m\Omega}$	**CERAMIC** $\mathbf{C = 300\mu F}$ $\mathbf{ESR = 0.3m\Omega}$	**CERAMIC** $\mathbf{C = 30\mu F}$ $\mathbf{ESR = 3.3m\Omega}$
VM	medium	medium	good	good	good	good
$\mathbf{V^2}$	excellent	bad	bad	bad	bad	bad
$\mathbf{V^2I_c}$	excellent	excellent	excellent	excellent	very good	excellent

V. Summary and conclusions

An optimization algorithm to design the control of power converters for a very fast and robust dynamic behavior has been proposed and validated in simulation and in an experimental prototype. Using the algorithm, the optimized transient responses of Voltage mode, V^2 and V^2I_c have been compared under different output capacitors: a $300\mu F$ OS-CON cap, a $300\mu F$ ceramic cap and a $30\mu F$ ceramic cap. As optimized controls are compared, the study is very meaningful. Table I shows a summary of the comparison.

As a result of the comparison, several conclusions have been drawn:

- V^2I_c is a very appropriate control in order to achieve very fast and robust dynamic response under load disturbances and voltage reference steps.
- If high-ESR capacitors are used and the application does not require voltage reference tracking, V^2 control is preferable because of its simplicity.
- As opposed to V^2I_c, the dynamic performance of Voltage mode control is constrained by robustness issues. Voltage mode needs to be designed slower in order to maintain stability regarding the range of variation of the passives of the power stage due to tolerances.
  For closed systems where the power stage is not susceptible to be changed by the end-user and the tolerances of the passive elements are very narrow, the converter is inherently robust. For these cases, Voltage mode control can be preferable, achieving very similar results as V^2I_c.

This means that, in order to achieve a very fast dynamic response, a traditional Voltage mode control can be sufficient if the tolerances of the system are narrow. However, if the tolerances are wide, which is the typical case, V^2I_c is preferable.

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